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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Rajski et al.
Application No. 10/781,031
Filed: February 17, 2004
Confirmation No. 2828
For: METHOD FOR SYNTHESIZING LINEAR FINITE STATE MACHINES
Examiner: David H. Malzahn
Art Unit: 2193
Attorney Reference No. 1011-67627-01

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Listed on the accompanying form PTO-1449 and enclosed herewith are several English-language documents. Applicants respectfully request that these documents be listed as references cited on the issued patent.

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Respectfully submitted,

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Docketing

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Attorney Docket Number	1011-67627-01
Application Number	10/781,031
Filing Date	February 17, 2004
First Named Inventor	Rajski
Art Unit	2193
Examiner Name	David H. Malzahn

U.S. PATENT DOCUMENTS

Copies of U.S. Patent documents do not need to be provided, unless requested by the Patent and Trademark Office. For patents, provide the patent number and the issue date. For published U.S. applications, provide the publication number and the publication date. For unpublished pending patent applications, provide the application number and the filing date.

Examiner's Initials*	Cite No. (optional)	Number	Publication Date	Name of Applicant or Patentee
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		6,308,291	10.23.2001	Kock et al.

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Examiner's Initials*	Cite No. (optional)	Country	Number	Publication Date	Name of Applicant or Patentee

Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS
		Aitken et al., "A Diagnosis Method Using Pseudo-Random Vectors Without Intermediate Signatures," *Proc. ICCAD*, pp. 574-577 (1989).
		Bardell et al., Built-In Test for VLSI Pseudorandom Techniques, Chapter 4, "Test Response Compression Techniques," John Wiley & Sons, Inc., pp. 89-108 (1987).
		Benowitz et al., "An Advanced Fault Isolation System for Digital Logic," *IEEE Transactions on Computers*, Vol. C-24, No. 5, pp. 489-497 (May 1975).
		Chakrabarty et al., "Optimal Zero-Aliasing Space Compaction of Test Responses," *IEEE Transactions on Computers*, Vol. 47, No. 11, pp. 1171-1187 (November 1998).
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EXAMINER SIGNATURE:	DATE CONSIDERED:

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	Art Unit	2193
	Examiner Name	David H. Malzahn

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		Ghosh-Dastidar et al., "Fault Diagnosis in Scan-Based BIST Using Both Time and Space Information," *Proc. ITC*, pp. 95-102 (September 1999).
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		Kundu, "On Diagnosis of Faults in a Scan-Chain," *Proc. VLSI Test Symp.*, pp. 303-308 (1993).
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		Wu et al., "Scan-Based BIST Fault Diagnosis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 2, pp. 203-211 (February 1999).

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